SPECIFICATIONS
NIM Model 3001
qVt MULTICHANNEL ANALYZER

GENERAL OPERATIONAL CHARACTERISTICS

Analysis Modes:

Q: Current integrating (charge sensitive); integration interval 20 nsec to 1 μsec; full scale, 256 pC ± 10% sensitivity, 0.25 pC/channel.

V: Peak voltage; input signal risetime, ≥ 50 nsec; full scale, + 1 volt or + 10 volt ± 10%; resolution, 1 mV or 10 mV/channel; external gate width, 100 nsec minimum to 1 μsec or switch selectable 5 μsec maximum.

T: Time interval (Start/Stop); full scale internally switch-selectable, 102 or 1024* nsec ± 10%; resolution, 100 psec and 1 nsec respectively.

Number of Channels:

1024 (10-bits); 256 (8-bits) in quadrants; overflow counts are stored in the last address of the selected memory segment.

Memory Size:

16 bits – 1 per channel (65,535 counts).

Digitizing Time:

12 μsec + 0.05 μsec/channel.

Temperature Stability:

± .03% of full scale/°C.

Long-Term Stability:

± 0.2% of full scale/week, maximum.

Integral Non-linearity:

± 0.25% of reading ± 2 channels.

Display:

100 sweeps/second

Channel Intensification:

Every 10th or 50th channel, front-panel selectable.

PHYSICAL CHARACTERISTICS

Packaging:

#2 width, RF-shielded NIM-standard module, conforming to specifications outlined in AEC Report TID-20893.

Voltages Used:

± 24 volts, ± 12 volts (Note: a rear-panel switch permits operation from ± 6 volts (if available) instead of ± 12 volts.)

Current Requirements:

+ 24 V at 24 mA	– 24 V at 125 mA
+ 12 V at 06 mA	– 12 V at 127 mA
+ 6 V at 1.35 A	– 6 V at 510 mA

Note: ± 6 V requirements add to ± 12 V requirements when ± 6 V option is unused.

Front-Panel Connectors:

BNC.

INPUT CHARACTERISTICS

Analog Input (Q and V Modes):

Direct-coupled; impedance, 50 Ω optionally, 93 Ω in V mode; protected to ± 100 volts for 1 μsec; linear range, 0 to – 1 volt in Q mode, 0 to + 1 volt in V mode.

External Gate/External Trigger/ Start/Internal Gate View:

One Common front-panel connector; functionally controlled by trigger mode switch; requires – 600 mV signal into 50 Ω.

Q and V Modes: In External Gate (EXT. GATE) mode, the gate width is equal to the duration of the gate pulse applied to this connector.

In External Trigger mode (EXT. TRIG), the internal gate is triggered by the leading edge of a fast NIM signal applied to this connector (min. trigger width, 10 nsec).

In Internal (INT) mode, the internally-generated gate may be viewed at this connector. Amplitude ~ 100 mV.

Q Mode: Usable gate duration, 20 nsec to 1μsec.

V Mode: Minimum duration, 100 nsec. Maximum duration, 5 μsec. (Gate must enclose peak of input signal to be measured.)

T Mode: The leading edge of Start input begins the start-stop time measurement; minimum pulse width, 10 nsec. External trigger mode only.

Inhibit/Stop:

One common front-panel connector; requires – 600 mV into 50 Ω.

Q and V Modes: Conversion is inhibited by application of a NIM inhibit signal. This level must be established before, and persist at least 20 nsec after the leading edge of the gate trigger. Inhibit is ignored after conversion is begun.

T Mode: Leading edge of stop pulse terminates the interval measurement; minimum pulse width, 10 nsec.

FRONT PANEL CONTROLS

Gate Width

Front-panel multiturn gate width control for Internal and External Trigger mode operation with range of 20 nsec to 1 μsec (5 μsec switch-selectable in longer time range). Setting stability ± 1% or 1 nsec, whichever is greater. Output monitors permit switch-selectable viewing of internal gate pulse for precise adjustment. Lower level discriminator triggers internal gate.

*Range 120 to 1120 nsec.

Threshold: Front-panel screwdriver-adjustable potentiometer determines threshold setting in internal trigger (INT) mode. Range, −1 mV to −15 mV in Q mode, +1 mV to +15 mV in V mode. Front-panel monitor point gives output voltage equal to 1000X actual threshold setting. Threshold stability <0.2%/°C over 20°C to 60°C operating range.

Operating Mode: One of the three analysis modes (Q, V, or T) is selected by a 3-position switch.

Trigger Mode: A 3-position switch selects internal trigger operation (INT), External Trigger operation (EXT TRIG), or operation via an externally-applied gate pulse (EXT GATE).

Continuous/Stop at Overflow: A 2-position switch either permits continuous data collection and display or limits each channel to a full scale capacity.

Intensify: Either every 10th or every 50th channel is intensified on the display, determined by a front-panel 2-position switch.

Display LIN/LOG: Selects linear or logarithmic display.

Start/Stop: Front-panel two-position, spring-return toggle switch. Start position initiates new measurement cycle after a Stop or Clear. Stop position stops measurement cycle.

Clear: Front-panel spring-return toggle clears all memory and register. Start/Stop switch must be simultaneously placed in stop position.

Memory Select:
Full-¼-²⁄₄-³⁄₄-⁴⁄₄ In the Full position, all 1024 channels accept and display input data.

In the ¼ position, the first quadrant (256 channels) accepts and displays input data. Full-scale range settings remain the same (i.e., 256 pC, +1 volt, and 102 or 1024 nsec); similar for ²⁄₄, ³⁄₄, ⁴⁄₄.

Vertical Gain: In LIN (linear) mode, an 8-position switch selects a maximum number of counts to be displayed per channel, between 512 and 65 k.

FRONT PANEL INPUTS

Q Input: Analog input; 50 Ω impedance; dc coupled. Accepts input charge of 0 to 256 pC. Protected to ± 100 volts.

V Input: Analog input 50 Ω impedance (93 optional). Accepts input voltage of 0 to +1 V (with switch selection 0 to 10 V range). Protected to ± 100 volts.

Gate Input/Output: Multifunctional connector. Acts as trigger or gate input/output in Q or V mode. Acts as start input in T mode. Input impedance 50 Ω. Accepts NIM fast signals. (See detailed specifications.)

Inhibit/Stop Accepts fast NIM signals. Acts as inhibit in Q or V mode and stop input in T mode. Impedance 50 Ω.

FRONT PANEL OUTPUTS

Threshold Test Point: Reads 1000X preset threshold value in Internal mode operation.

Internal Gate View: Internally generated gate is available for oscilloscope monitoring on the Gate Connector when Internal Trigger is selected. Amplitude: −100 mV.

Internal Gate Test Point: Internally-generated gate is available for oscilloscope monitoring when Internal or External Trigger mode is selected. Amplitude: −200 mV.

Busy: TTL low level output during conversion time.

Horizontal Out: Horizontal deflection voltage for CRT proportional to channel number; 0-5 volts for full or quadrant display. Minimum load impedance 1 kΩ.

Vertical Out: Vertical deflection voltage for CRT proportional to number of counts. Linearity ±0.2% of full scale. Full-scale output of 5 volts corresponds to 200 db/volt in the log mode. Minimum load impedance 1 kΩ.

REAR PANEL OUTPUTS

Connector Type: 44-contact card-edge connector; mates with AMP 582358-2 (hood number 530087-4).

Memory Overflow (22): A high TTL level* indicates channel overflow. Available during memory load only.

External Enable (4): Low TTL level* enables external functions accessed by the rear connector.

External Memory Address Latch (R): The trailing edge of a positive-going TTL-compatible* pulse of minimum duration 200 nsec. latches the address applied to the 10 Memory Address lines (A,B,C,D,E,F,G,H,J,K,L), corresponding to 2^0 to 2^9 respectively.

Memory Enable (21): TTL-Compatible high level* causes the contents of the memory address latched in lines A-L to be loaded into the internal incrementing register. A low level permits loading of the 16-External Data Input levels** into the Incrementing Register.

**Pin 6 : 2^0	Pin 10 : 2^4	Pin 14 : 2^8	Pin 18 : 2^{12}
5 : 2^1	9 : 2^5	13 : 2^9	17 : 2^{13}
7 : 2^2	11 : 2^6	15 : 2^{10}	19 : 2^{14}
8 : 2^3	12 : 2^7	16 : 11^{11}	20 : 2^{15}

External Load (N): A low level* latches the Internal Incrementing Register. Data must be quiescent during load interval. Minimum duration 200 nsec.

External Read/Write (M): Causes data to be read from the memory to the Internal Incrementing Register or written in memory from the Internal Incrementing Register. Low for read, high for write.*

Incrementing Register (P): Leading edge of positive-going TTL level causes the contents of the incrementing register to be incremented by 1.

*TTL levels Low: −0.8 V; High −2.0 V

SPECIFICATIONS SUBJECT TO CHANGE.